

One to Five Cell Li-Ion Charger-IC N μ 701.65A

Including Load-Management

Packs with **1 – 5 Cells** may be charged. All voltage-levels can be adjusted to the Lithium-systems needs. Voltage levels are adjustable to various chemistries like Lithium-Manganese, LiFePO, Li-Polymer etc.

The IC **includes a Step-Down switching regulator** for charging a cell-stack from a wall adaptor. While charging, the IC monitors the voltage of each cell.

Unequal cell-voltages are leveled by **balancing**.

If any cell voltage drops below the minimum voltage the **load is cut off**.

For EMC-reasons the load is cut off when the wall adaptor is plugged in.

The IC ensures by **temperature monitoring** that charging is only possible within the approved temperature range.

Two Status-LEDs are used to display charge condition and error-codes.

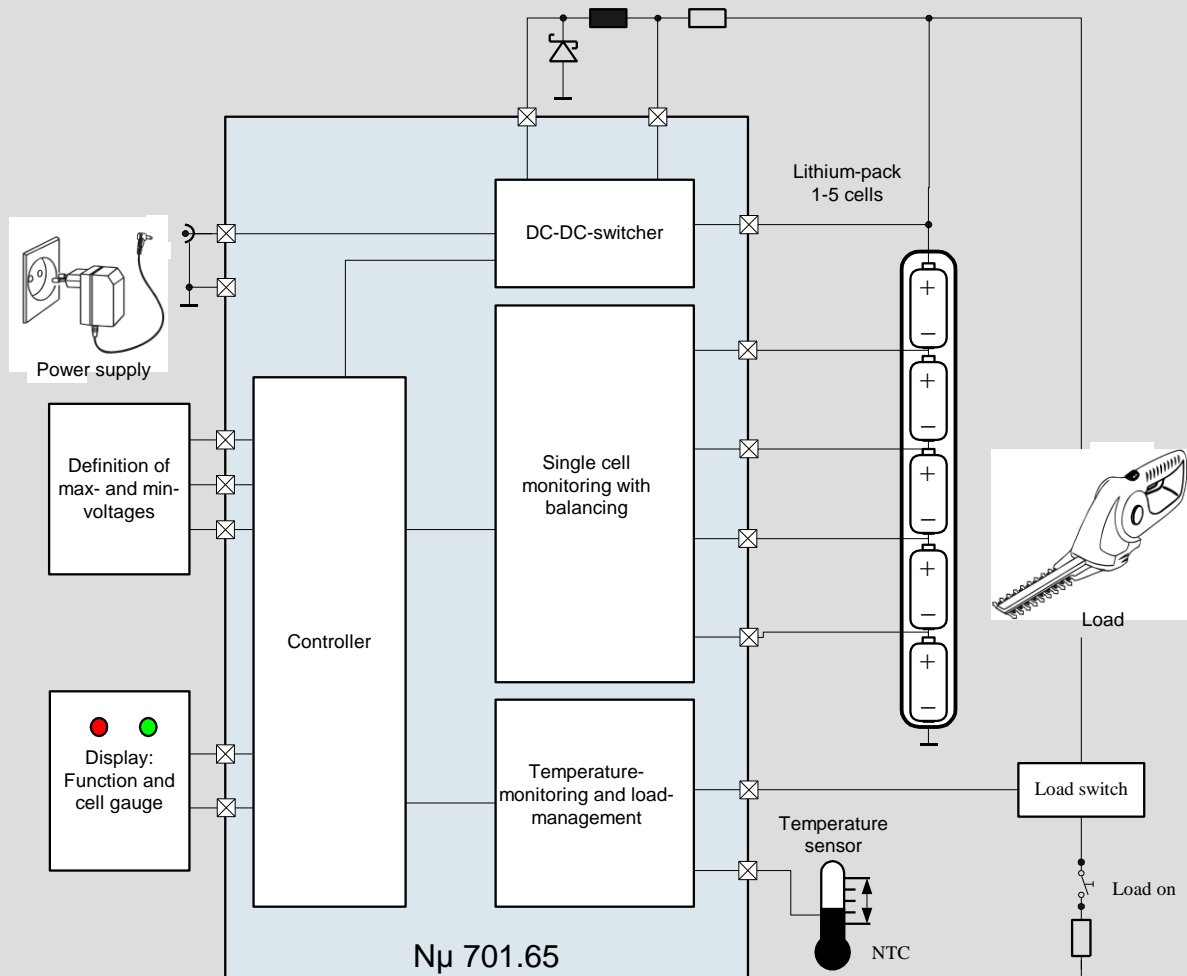
Internal status-registers can be read via SPI. Besides the stand-alone-mode, the whole charging process can be managed by an external Microcontroller optionally.

Features:

- Single Cell Voltage Monitoring
- Charge-Balancing
- Adjustable Voltages
- Integrated Switching Regulator, EMC-optimised
- Temperature Monitoring
- Charge & Load Management
- C/5 Charge Termination

Applications:

- Power Tools
- Gardening Equipment
- Emergency Lighting
- Portable Equipment

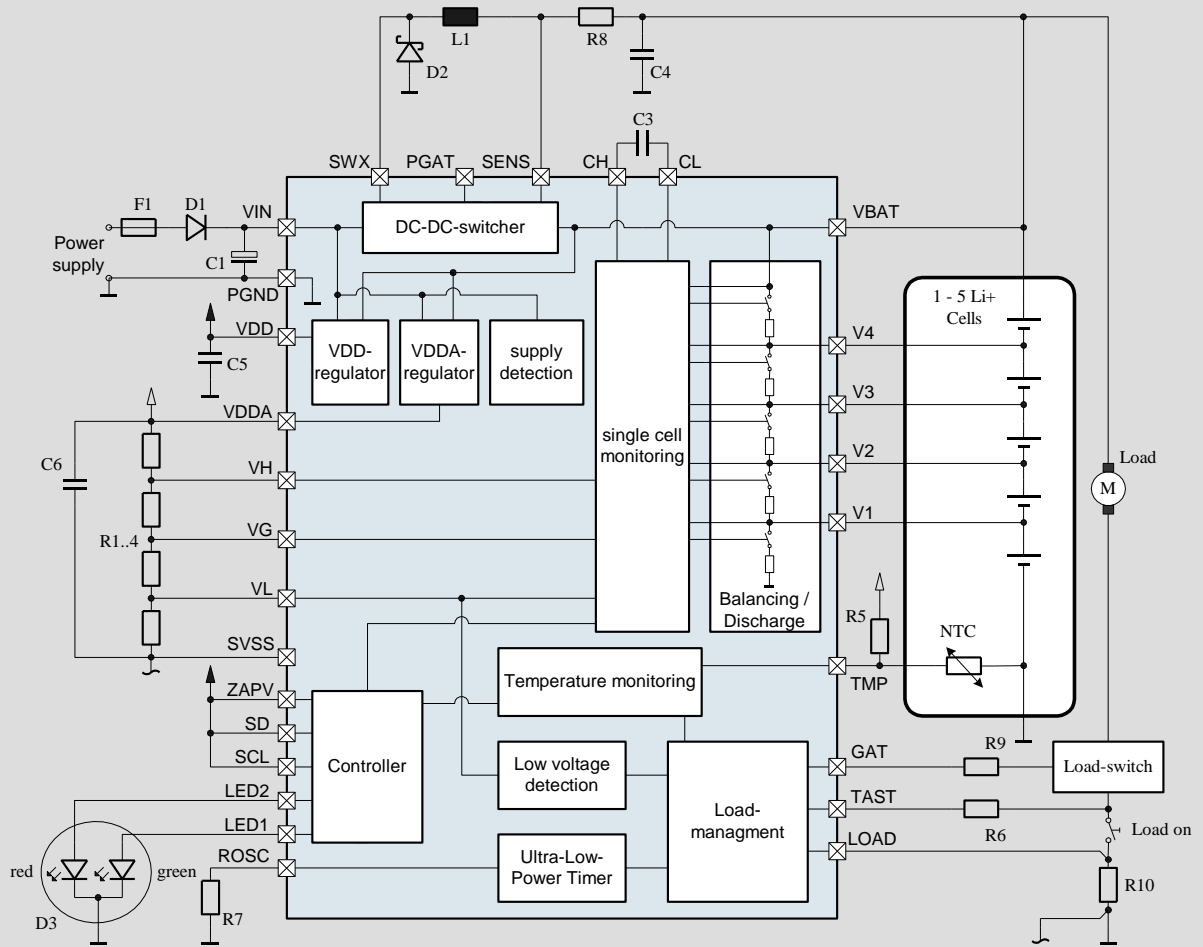


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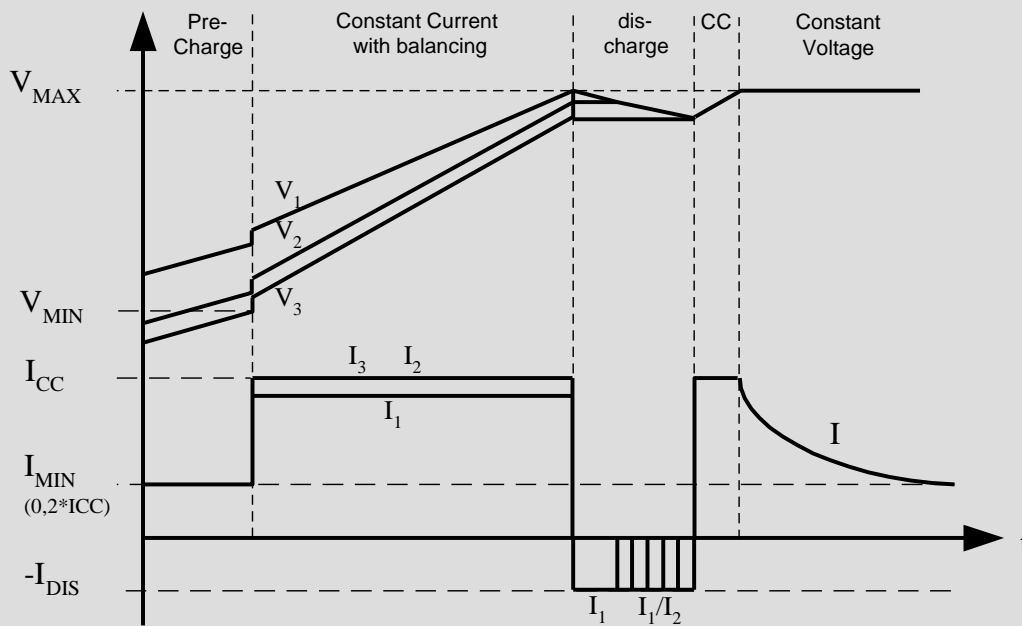
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1.1 Block Diagram



1.2 Charge Cycle

The IC supports the constant-current / constant-voltage method (CC/CV) including a precharge-phase in case of deep discharge. The charging consists of five cycles defined by the voltage levels V_{MIN} and V_{MAX} , and the currents I_{MAX} , I_{MIN} and I_{DIS} . The charge cycle runs entirely automatic and is indicated by flashing of the green LED. The following example shows charging of a discharged battery with three unbalanced cells.



1.2.1 Precharge-Phase (PreC)

If one cell voltage of the pack is below V_{MIN} (deep discharge), the pack is charged with the minimum current I_{MIN} , until every cell exceeds V_{MIN} . Then deep discharge is overcome and the battery is preconditioned for the CC/CV charging-method.

1.2.2 Constant-Current-Phase with Balancing (CC)

Charging enters the CC-Phase if each cell voltage is above V_{MIN} and below V_{FULL} . The battery is charged with I_{MAX} , and the cell voltages are rising with charging level. The battery obtains 80% of its total charge during this phase. The CC-phase ends, when one cell reaches V_{MAX} . Balancing is accomplished by reducing the charge-current of the cell with the highest voltage (see chapter 1.6).

1.2.3 Discharge-phase

If the battery is still unbalanced after CC-charging with balancing, the cells with the highest voltages are identified and discharged one by one with I_{DIS} . Discharge is terminated when all cell voltages are equal or one cell-voltage is below V_{MIN} .

1.2.4 Constant-Current-Phase 2 (CC2)

This phase is equal to the first CC Phase. The amount of charge lost during discharge phase is replaced.

1.2.5 Constant-Voltage-Phase (CV)

The battery obtains its full charge by fixing the voltage of the fullest cell at V_{MAX} . While charge increases, the current is lowered. The battery is fully charged when the charging current drops below I_{MIN} , current is cut off and charging is terminated.

1.2.6 Re-charging by connecting charge-supply to the mains

The voltage of each cell must be below the charge-limit V_{FULL} for charging to start. A cell-pack is considered to be fully charged if one cell is above V_{FULL} and all other cells are at least above V_{MIN} . V_{FULL} is the voltage at VH with the internal load resistor R_{LAST} switched on. (see chapter 1.3)

1.2.7 Re-charging when charge-supply stays connected

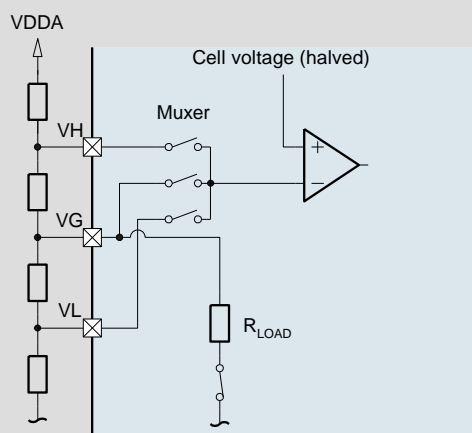
In case the charge-supply stays connected to the mains after charging is terminated, each cell-voltage will be checked in time intervals T_{NL} or after closing the load-switch. If one cell-voltage is below the recharge-limit V_{NL} a new charging cycle is started.

1.2.8 Charging of deep-discharged or defective cells

In case a cell-defect is recognized, the circuit tries to charge for several minutes (T_{TO_DEF}) with the lowest current I_{MIN} . If the defect is still present after T_{TO_DEF} charging will be terminated and a battery-error will be signaled. (see chapter 1.10.2)

1.3 Voltage levels during charging

Maximum cell voltage:	V_{MAX}	= 2 x V(VH)
Charge-limit:	V_{FULL}	= 2 x V(VH _(RLOAD on))
Recharge-limit:	V_{NL}	= 2 x V(VG)
Minimum cell voltage:	V_{MIN}	= 2 x V(VL)



1.4 Timeouts

All Timeouts are T_{T0} hours. Timer is reset to zero at the beginning of each charging-phase

Precharge-Phase (PreC) Timeout

Precharge-phase will be terminated latest after T_{T0} hours. If one cell is then still below V_{MIN} there will be a timeout-signal (red flashing).

Constant-Current-Phase (CC) Timeout

CC is terminated latest after T_{T0} hours. If no cell has reached V_{MAX} until then, there will be a timeout-signal (red flashing) and charging will be terminated.

Discharge-Phase Timeout

Discharging will be terminated latest after T_{T0} hours and the 701.65 will proceed to CC2.

Constant-Current-Phase 2 (CC2) Timeout

CC2 is terminated latest after T_{T0} hours. In case no cell has reached V_{MAX} until then, there will be a timeout-signal (red flashing) and charging is terminated.

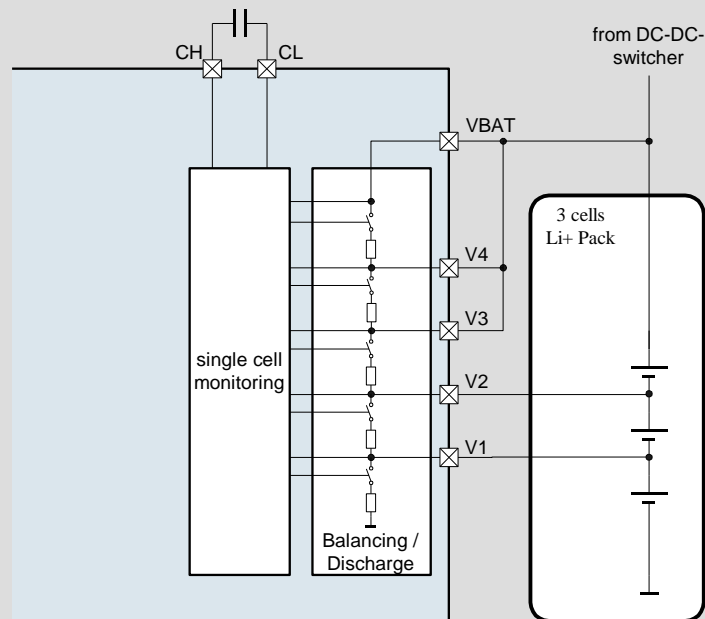
Constant-Voltage-Phase (CV) Timeout

CV is terminated latest after T_{T0} hours. If the charge current has not dropped below I_{MIN} until then, there will be a timeout-signal (red flashing) and charging is terminated.

1.5 Determining Cell Count

A cell pack consists of a single cell or a series connection of 2 to 5 cells. Parallel connections of cells will be treated as one cell. The positive terminal of cell one to five is connected to the voltage-sense-pins V1-V4 and VBAT respectively. With a cell pack of less than 5 cells the unused voltage-sense pins must be connected to V_{BAT}, starting with V4.

The 701.65 determines the cell count during precharge-phase by measuring the voltage between VB/V4, V4/V3, V3/V2, V2/V1 and V1/VSS. If the voltage between these sense-pins is below V_{SHORT}, the 701.65 assumes that there is no cell and the sense-pins are shorted. The following example shows the circuit for three cells.



1.5.1 Detection of Cells with Reversed Polarity

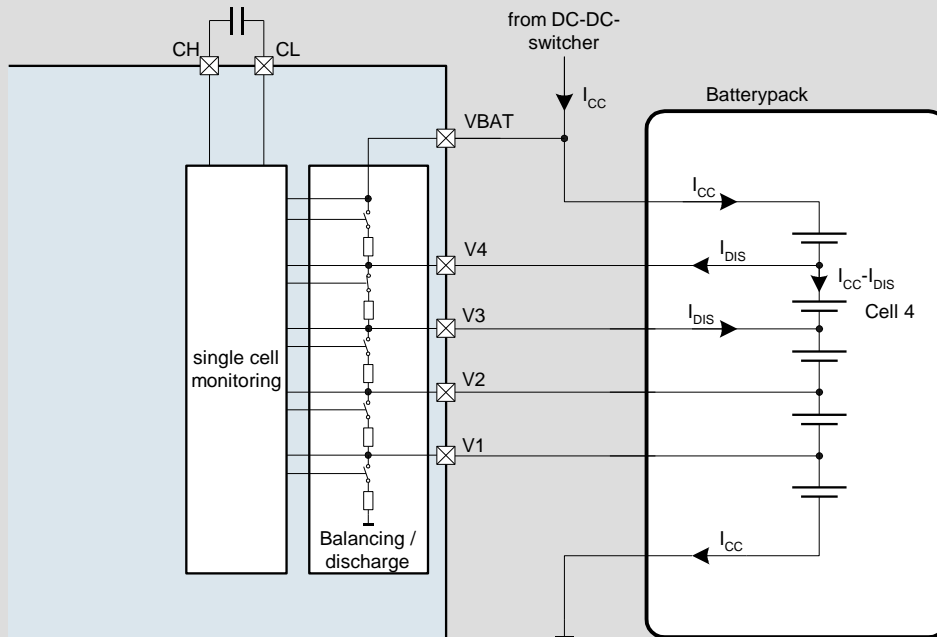
Under certain circumstances damaged cells may reverse their polarity. A cell-error is detected if a cell-voltage is below $-U_{SHORT}$. After a delay of T_{OFF} the load-switcher will be turned off and battery-error is signaled (red flashing).

1.6 Balancing

Balancing is a measure to accomplish full charge of each cell even if their state of charge is different at the beginning. Therefore in the constant-current phase a part of the charge current I_{CC} of the cell with the highest voltage is diverted (I_{DIS}).

During discharge-phase the cell with the highest voltage is discharged with I_{DIS} .

The following example shows a 5-cell-pack during constant current phase where the 4th cell has the highest voltage.

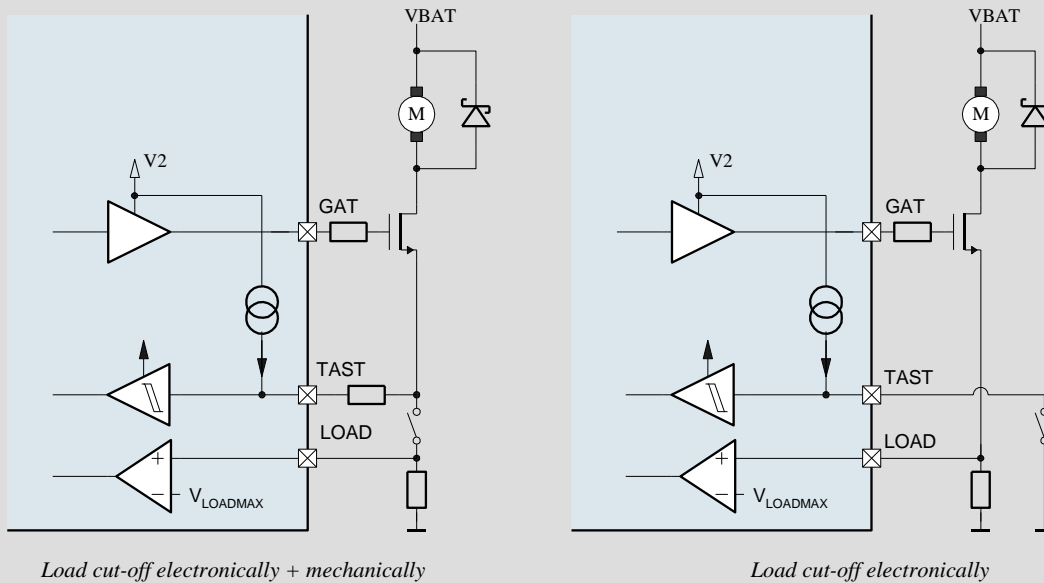


1.7 Load Driver and Switch Input

GAT is an output to drive an external transistor which enables the 701.65 to control the load of the cell-pack. The load will be disconnected if any cell drops below V_{MIN} or in case the temperature is out of the allowed range. To avoid EMI, the load is also cut off when the charge supply is been connected.

The switch input TAST detects whether the switch is closed by the user. It may be connected in two ways:

1.7.1 Examples for Load Driving



The on-voltage of GAT is equal to the voltage at pin V2 which is the positive terminal of the second cell with respect to ground. In case there is only one cell, a transistor with an appropriate low threshold voltage has to be used.

1.7.2 Determining switch status

Input TAST is an active low Schmitt-trigger input with pull-up. „Switch closed“ will be determined, if the voltage at TAST falls below V_{SG} .

1.8 Load management

The cell pack is protected from deep-discharge as well as over- and under-temperature operation when the load is switched on.

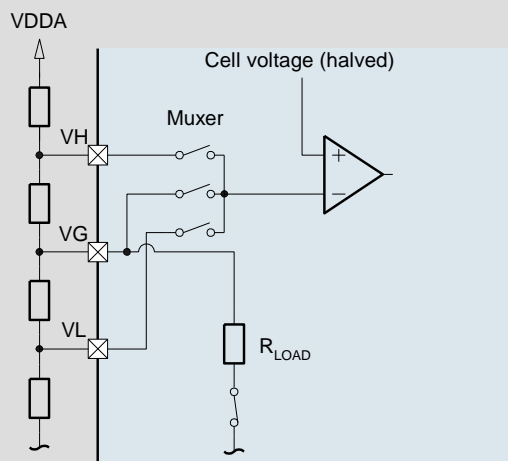
1.8.1 Voltage levels during load on

During load on each cell voltage is monitored constantly to protect the cells from under voltage and to display cell gauge.

Therefore cell voltages are divided by 2 and compared with VG (with R_{LOAD} pull down turned on) and VL.

Accumulator low: $V_{\text{YELLOW}} = 2 \times V(\text{VG}_{(\text{R}_{\text{LOAD}}=\text{on})})$

Minimum Cell Voltage: $V_{\text{MIN}} = 2 \times V(\text{VL})$



State of charge high

If each cell voltage is above V(VG) after the load has been turned off, the LED shows green light for the time T_{LED}.

State of charge low

If any cell voltage is below V(VG) after the load has been turned off, the LED shows yellow light for the time T_{LED} signaling charging will be necessary soon.

1.8.2 Temporary and actual deep discharge

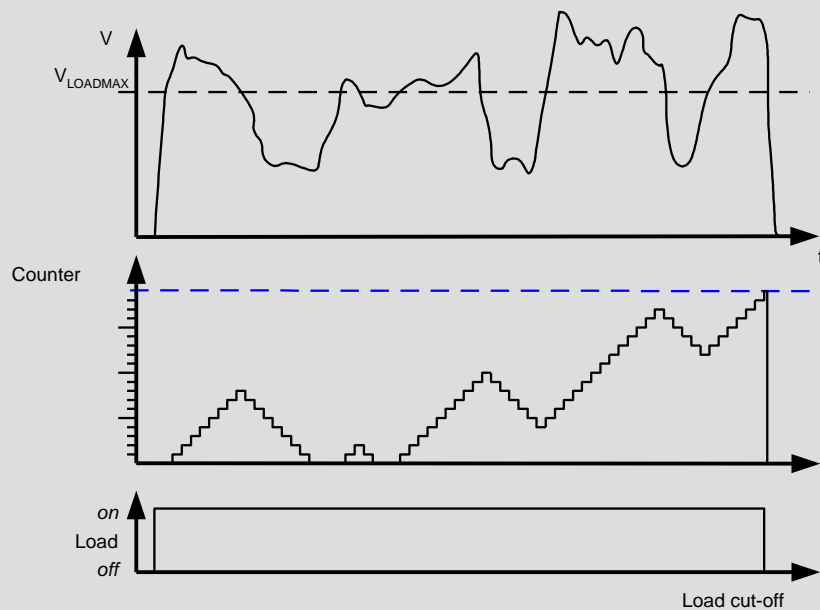
If any cell voltage drops below the deep discharge limit $V_{\text{MIN}} = 2 \times V(\text{VL})$ during load on for longer than T_{OFF}, the load is turned off and the LED shows red light for the time T_{LED}. Typically the cell voltage recovers somewhat after the load is removed and it rises above V_{MIN}. Now the 701.65 has to decide whether there was a short overload or the battery is really almost empty. If all cell voltages are above V_G x 2 next time the TAST switch is closed, a green light signals the possibility to continue work with the device. If the battery cells do not recover above V_G x 2, a red LED signals that it is not possible to use the device before recharge.

After the load was shut off by the load management, the 701.65 will always wait for the user to release the switch, before the load is enabled again.

1.8.3 Overload Shut Off

Load current is measured through the shunt R10. Short time overloads must not lead to shutdown of a power tool. It should instead powerfully overcome any temporary resistance. If such an overload occurs for too long or repeatedly, it may damage the equipment.

If the load current exceeds the desired value, a 19-stage counter counts with T_{CL_LOAD} upward. If the load current drops below this limit the counter counts down with T_{CL_LOAD} . Therefore short overloads will be ignored. At multiple surpassing of the overload threshold with only short breaks, the counter counts upwards and the load is switched off as the counter reaches its maximum count. With a continuous overload condition the load is switched off after the time T_{OL} . Once the load was switched off, it may be turned on again after the Time T_{OL} . The desired current limit may be chosen by the value of the shunt-resistor R10.

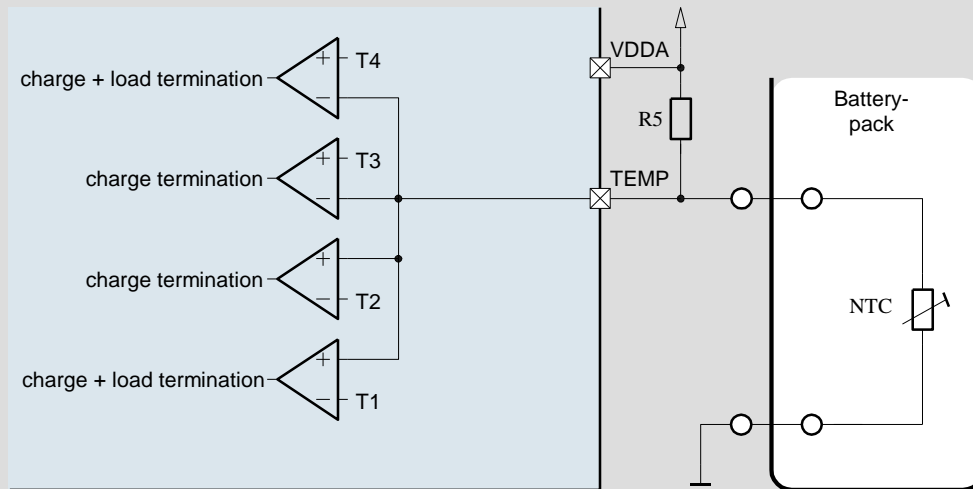


1.8.4 Short-Circuit-Protection

In case of short-circuit, the very high current may cause damage to the device. Therefore in this case the load has to be turned off fast. If the voltage at pin LOAD exceeds the value of five times $V_{LASTMAX}$ the load will be turned off within T_{SC} . Once the load was switched off, it may be turned on after the Time T_{OL} .

1.9 Temperature Monitoring

To ensure operation within the appropriate temperature range, the 701.65 has a pin TEMP to connect an external temperature dependant resistor (NTC).



There are four temperature thresholds being monitored. A temperature error will be signaled if a limit is being violated for a time longer than T_{OFF} . In the following example R5 is 4k7 Ω and the NTC is 6K8 Ω @25 $^{\circ}$ C, Vishay 2381 640 6 3682:

- T1 (-20 $^{\circ}$ C):** The actual temperature is below the operating temperature of the battery-cell. Load will be disconnected, charging is disabled.
- T2 (-5 $^{\circ}$ C):** The actual temperature is below the charging temperature of the battery-cell. Charging is disabled.
- T3 (45 $^{\circ}$ C):** The actual temperature is above the charging temperature of the battery-cell. Charging is being terminated.
- T4 (65 $^{\circ}$ C):** The actual temperature is above the operating temperature of the battery-cell. Load will be disconnected, charging is disabled.

If a temperature error occurs during operation (switch at TAST on) for longer than T_{OFF} , the load will be disconnected and a yellow LED will flash for T_{LED} . When the switch at TAST is closed the next time, the temperature is being checked. Is the temperature within the operating temperature range and each cell-voltage above $V(VG) \times 2$, a green LED will come on. After opening the TAST switch, the load will be enabled again. If there is a temperature error during less than T_{OFF} , there will be a warning by a yellow LED after the TAST switch is opened. Load stays enabled until a temperature error occurs for longer than T_{OFF} .

Short temperature error during operation are not being signaled.

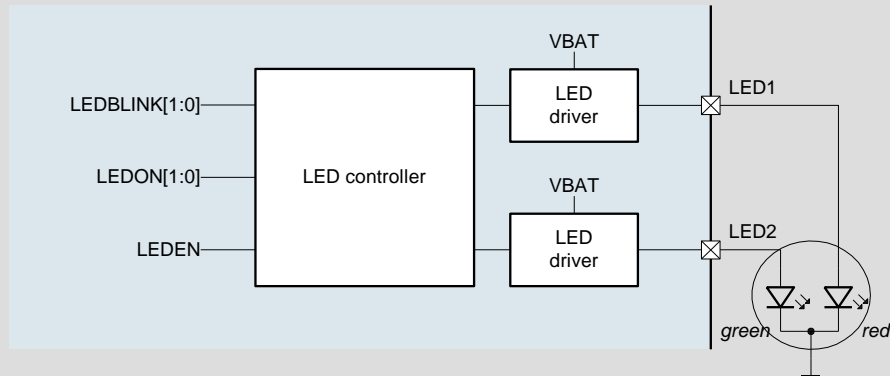
After a temperature error during charging with the charging supply connected the temperature will be checked every T_{NL} and when the TAST switch is being connected. If the temperature is then within the appropriate range, charging will be restarted.

1.9.1 Disabling Temperature Monitoring

If no temperature monitoring is desired, the NTC and R5 are unused. The pin TEMP still has to be provided with a voltage between V_{T2} and V_{T3} . This can easily be achieved by connecting TEMP to VG.

1.10 Status-LEDs

The 701.65 handles two LEDs to display battery gauge and error codes by flashing or shining continually. Usage of a red/green DUO-LED shows a yellow color when both LEDs are on. The LEDs are off if the TAST switch is on.



1.10.1 Status Monitoring

- Charging: Green flashing
- Charging terminated: Green continuously on until charge supply is disconnected.
- At discharging (Load in use): Red: Load termination voltage reached. Load disabled.
- After TAST switch off for the time T_{LED} :
Green LED: Battery more than 50% capacity
Yellow LED: Battery less than 50% capacity
Red LED: Load termination voltage reached, battery empty

1.10.2 Error Codes

- Charging timeout: red flashing fast
- Battery error: red flashing slow
- Temperature error shorter than T_{OFF} : Yellow continually for T_{LED} after opening of TAST switch.
- Temperature error long than T_{OFF} : Yellow flashing slow.
- Motor error (overload): Yellow flashing fast.

A Battery error is displayed, if one cell voltage is below V_{MIN} and another has reached V_{MAX} , or if one cell voltage falls below V_{SHORT} .

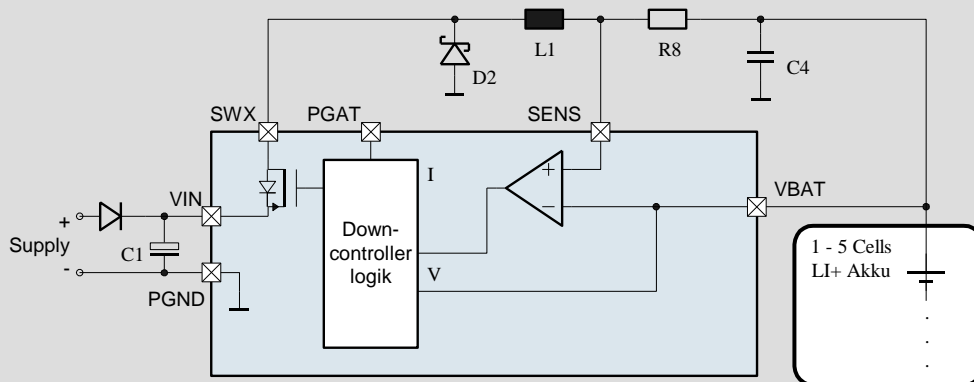
Status	Description	Color	Flash/Cont	Remark
1	Charging	Green	Flashing	Short pulse: PreC, CC, DIS-phase Long pulse: CV-phase
2	Charge finished (cells full)	Green	Cont.	Until charge supply is disconnected
3	Cells full (after switch is closed)	Green	Cont.	Duration: T_{LED}
4	Cells half (after switch is closed)	Yellow	Cont.	Duration: T_{LED}
5	Cells empty (after switch is closed)	Red	Cont.	Duration: T_{LED}
6	Timeout error	Red	Flashing	Fast f_{LEDf}
7	Cell Error	Red	Flashing	Slow f_{LEDs}
8	Temperature error for $<T_{OFF}$	Yellow	Cont.	Duration: T_{LED} after releasing switch
9	Temperature error for $>T_{OFF}$	Yellow	Flashing	Slow f_{LEDs}
10	Load error (overload / short circuit)	Yellow	Flashing	Fast f_{LEDf}

1.10.3 LED Driver LED1, LED2

LED1 and LED2 are current sources to drive two LEDs directly without a resistor. I_{LED} is drawn from VBAT.

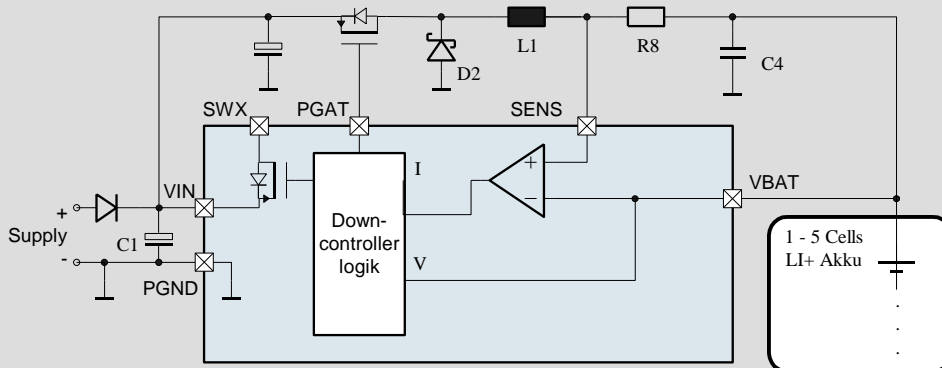
1.11 DC-DC Buck Converter

The 701.65 has an integrated Power-MOSFET as the central part of a down converter. The maximum output current is limited by the cooling of the chip and the current rating of the pins VIN and SWX and is controlled by the shunt R8. External parts are an inductor, a Schottky freewheeling diode, a capacitor and a shunt resistor. Traces to the external parts have to be short due to the high switching frequency. The input capacitor has to be placed near the VIN-Pin, the freewheeling diode has to be placed near the SWX pin. The ground-connections of the input and output capacitor and the diode have to be routed very shortly and star-shaped. Connect the PGND-pin to the star-point.



1.11.1 DC-DC Down Converter with External FET

For higher charge current an extra p-channel mosfet controlled by the output PGAT may be used. Charge current is still controlled by R8.



1.11.2 DC-DC Down Converter Parameters

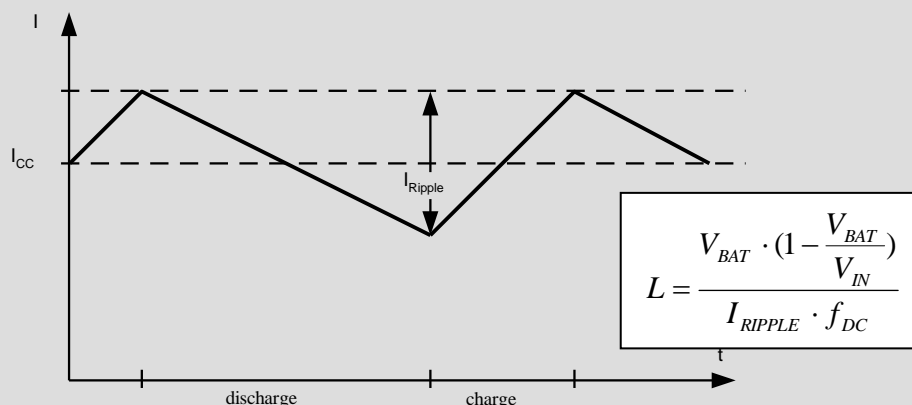
- I_{CC} : Average charge current during Constant-Current-Phase
- V_{SENS} : Voltage across the loading current shunt R8.
- I_{RIPPLE} : Ripple of the inductor current
- f_{DC} : Switching frequency of the regulator

1.11.3 Selecting Charge Current

Maximum charge current I_{CC} is determined by the value of the shunt resistor R8. The voltage across R8 is internally compared to V_{SENS} . If the internal power FET between VIN and SWX is used, the charge current must not exceed I_{CCMAX} .

$$I_{CC} = \frac{V_{SENS}}{R_{Shunt}}$$

1.11.4 Selecting the Inductor and Calculating the Current Ripple



The inductance should be selected that the regulator always is in continuous current mode. Therefore the current ripple has to be much smaller than I_{CC} . The current rating (saturation current) of the inductor has to be higher than $I_{CC} + 1/2 \times I_{RIPPLE}$.

1.11.5 Charge Current Regulation in the CV-Phase

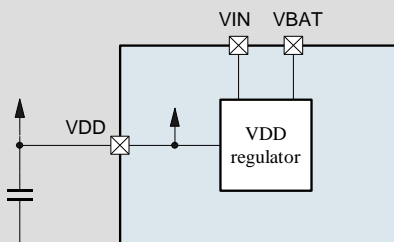
In the CV-phase the charge current is set so that none cell voltage exceeds V_{MAX} . Therefore with increasing charge the current becomes smaller until it drops below I_{MIN} and charge termination is reached. I_{MIN} is 20% of I_{MAX} , and is also determined by the shunt resistor R8. Charge termination current and precharge current are identical. The balancing current is independent of both.

1.11.6 Input Short Circuit and Reverse Polarity Protection

Due to technological reasons the integrated power-MOSFET has a body diode through which VBAT is present at VIN. This input has to be protected against shorting and reverse polarity by a diode.

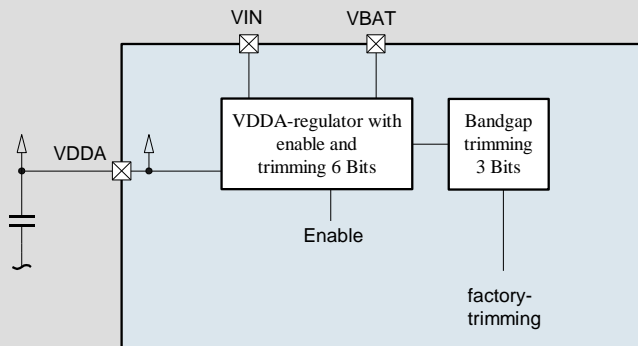
1.12 VDD

A linear regulator creates the internal supply-voltage VDD. The current is drawn either from the battery-voltage V_{BAT} or from V_{IN} .



1.13 VDDA

A linear regulator creates the internal analogue supply-voltage VDDA. VDDA is regulated exactly to supply the external voltage divider R1 .. R4, internal signals and an optionally connectable microcontroller. It has to be blocked by a 10 μ F Ceramic Capacitor from VDDA to SVSS.



1.13.1 VDDA-Activation

VDA A is enabled by the internal logic when either the charge supply is connected in or the TAST switch is closed. An optionally connected microcontroller supplied by VDDA will only be activated, when user-interaction requires supervision.

The 701.65 is awoken by the built in ultra-low-power-timer in intervals of T_{NL} while the charge supply is connected, to decide whether recharging is necessary.

1.13.2 VDDA-Deactivation

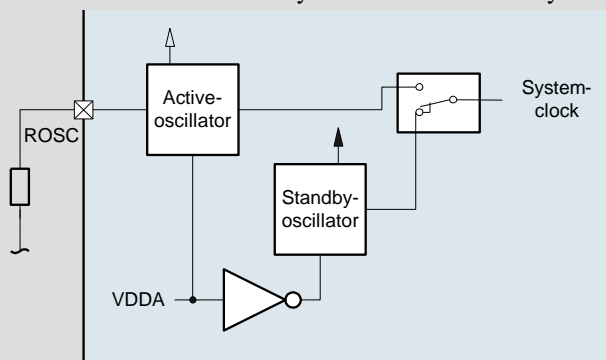
VDDA is deactivated to save battery life after end of charge or opening the TAST switch. If a microcontroller is used, it has to take care of deactivating VDDA.

1.14 Charge Supply Detection

A connected charge supply is detected if $V_{IN} > V_{BAT} + V_{NT}$. Is the supply being connected during TAST switch closed, load will be switched off within T_{OFF_NT} . After TAST switch is opened, charging begins.

1.15 Clock

The 701.65 has two different oscillators to provide the system clock. If VDDA is on, the fast active-oscillator is used. Otherwise the slow standby oscillator clocks the system.



1.15.1 Active-Oscillator

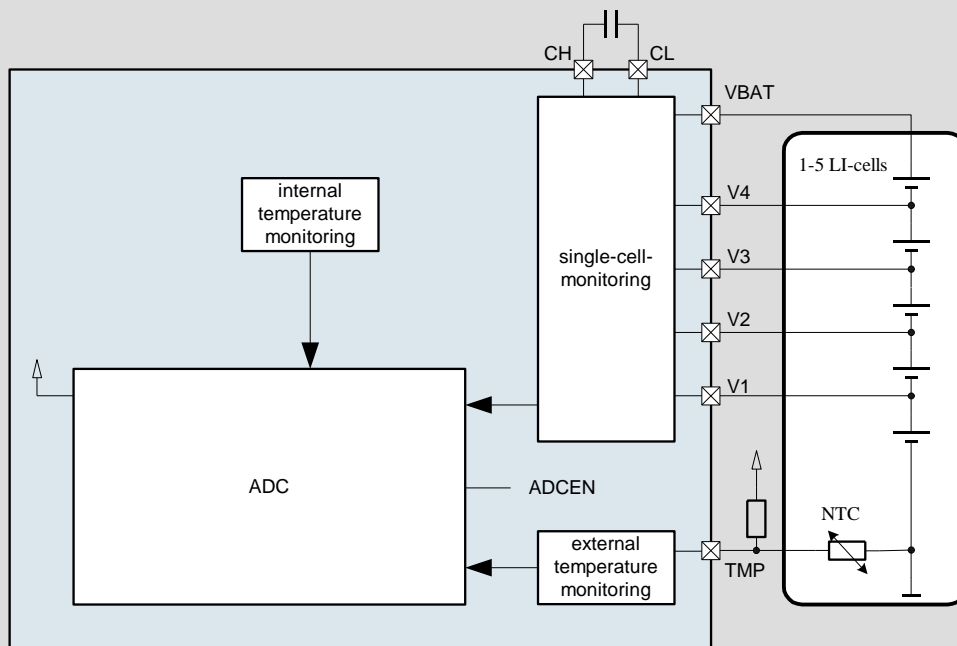
Internal oscillator for f_{OSCA} . Frequency may be adjusted by the resistor at ROSC.

1.15.2 Standby-Oscillator

The standby-oscillator supplies the systems clock whenever the active-oscillator is not running. The slow standby clock leads to considerably lower current consumption. The standby-oscillator may not be influenced from outside.

1.16 ADC

The 701.65 contains an 8 bit A/D-converter (ADC) with 6 Inputs and ENABLE. The ADC is supplied from VDDA and it is able to convert input-voltages from 100mV to VDDA-0.3V. The internal signal ADCEN turns the ADC on. The ADC converts the voltages at its inputs to 8 bit values and stores them in corresponding registers. After each conversion the ADC-Ready counter is incremented. The cell with the highest voltage is found out. In the registers ZGMAX, ZGGELB and ZGMIN is stored, which of the halved cell voltages are higher than the related threshold voltages V(VH), V(VG) and V(VL).



1.17 Microcontroller-Interface

The 701.65 can perform charge and load management as well as temperature monitoring without an external microcontroller.

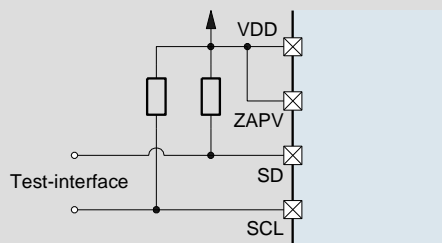
Through the two-wire-interface SD and SCLK a microcontroller can access and control the internal registers and in this way control the charge and load management. If a microcontroller is used, it has to manage the entire charge and load cycle, just changing some parameters is not possible. The two-wire-interface is described in the spate Application-Note AN701.65-115. There are also example-programs available in C (AN701.65-116) and National Instruments LabView (AN701.65-117).

1.17.1 Stand Alone

Stand alone operation without microcontroller is selected with the pins SD and SCL connected to VDD.

1.18 Zap-Cells

The internal voltage reverence is adjusted using zap-cells during final test in production. The zap-cells are accessed by the pins SD, SCL and ZAPV. In use ZAPV has to be connected to VDD. Subsequent adjustment is not possible.



2 Pin description

The following table shows pin-numbers, -names and -descriptions. Pin out differs between package variants.

PIN-# (QFN32)	Pin-# (SO28)	Name	Funktion
1	25	PGND	Power ground
2	--	nc	unused
3	26	V1	Positive terminal of bottom cell
4	27	V2	Positive terminal of second cell
5	28	V3	Positive terminal of third cell
6	1	V4	Positive terminal of fourth cell
7	2	VBAT	Positive terminal of top cell and battery
8	3	CL	negative terminal for level-shift capacitor
9	4	CH	positive terminal for level-shift capacitor
10	5	VDD	Internal digital supply voltage
11	6	ROSC	Pin for resistor setting the oscillator-frequency
12	7	SD	Data in/out for SPI
13	8	SCL	Clock in for SPI
14	9	ZAPV	Supply for zap-cells, connect to VDD
15	10	LOAD	Connect to load-shunt
16	11	SVSS	Analog-ground, connect to PGND
17	12	VDDA	Analog supply voltage
19	13	VL	Voltage divider lower terminal for V_{MIN}
18	14	VG	Voltage divider middle terminal for V_{YELLOW} and V_{NL}
20	15	VH	Voltage divider upper terminal for V_{MAX}
21	16	TMP	Connect to NTC for external temperature measurement
22	17	LED2	Green LED, current source
23	18	LED1	Red LED, current source
24	--	nc	unused
25	19	GAT	Gate driver for load-switch
26	20	TAST	Input for mechanical load-switch
27	21	SENS	Input for charge-current-shunt
28	22	PGAT	Gate driver for external charge P-MOSFET
29,30	23	SWX	Output of internal charge P-MOSFET
31,32	24	VIN	Charge-supply voltage (has to be protected against short-circuit and reverse polarity)
Cooling-pad	-	Cool	Connect thru 25 vias to big copper-area connected to SVSS

3 Absolute Maximum Ratings

Stress beyond those listed under “Absolute Maximum Ratings” even for a short time may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied.

Operating Voltage (VBAT-VSS)*	-0,3V ... 35V
Operating Voltage (VIN-VSS)*	-0,3V ... 35V
*: Condition: VIN>VBAT-0,3	
Maximum Input Current at VIN.....	1A
Maximum Output Current at SWX	1A
Input Current at V1, V2, V3, V4.....	-100 mA ... 100 mA
Input Current at VBAT	-100 mA ... 10 mA
Input Current at PGND	-10mA ... 100 mA
Input Current all other Pins	-10mA ... 10mA
Continuous Power Dissipation (P _{tot} , QFN32, T _A = 60 °C).....	4W
Storage Temperature Range (T _L)	-55°C ... 150°C
Junction Temperature Range (T _J) (Shut-Down 125°C).....	150°C
Operating Temperature Range (T _B).....	-25°C ... 125°C



3.1 ESD Protection

All standard pins are protected against damage by electrostatic discharge (ESD) according to MIL-STD-883C, method 3015.7 (100 pF 1,5 kΩ) for peak voltages up to +/- 2000V.

The application specific pins SWX, PGAT, LED1 and LED2 have different protection structures. Handling has to be done under careful observation of the appropriate handling rules for CMOS-devices. Externally accessible Pins have to be protected with additional protective circuitry.

3.2 Technology

Monolithically integrated CMOS-circuit. SI-Gate, n-well on epi substrate

	<p>Electrostatic Sensitive Devices</p> <p>Handling only under careful observation of the appropriate handling rules.</p>	
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4 Electrical Characteristics

All voltages related to SVSS; Supply voltage VBAT=20V, V_{VIN}=25V; fosc = 4,2MHz,
Temperature = 27°C unless otherwise indicated.

Parameter	Condition	Symbol	min	typ	max	Unit
Battery Voltage, Pin VBAT		V _{VBAT}	0		30	V
Supply Voltage, Pin VIN	U _{VIN} > U _{VBAT} +3V	V _{VIN}	8V		35	V
Switching Frequency Down-Converter	Continuous current mode	f _{DC}	450	525	600	kHz
Charge Current Charge	CC-Phase	I _{CC}			0,7	A
Charge Current Precharge	Precharge-Phase, End of Charge	I _{PRE}		0,2 x I _{CC}		
Balancing-Current	CC- und Discharge- Phase V(BAT)-U(V4)=3V V(V4)-U(V3)=3V V(V3)-U(V2)=3V V(V2)-U(V1)=3V V(V1)=3V	I _{DIS}	30	50	70	MA
Voltage across charge-current shunt	V(BAT) – V(SENS), Maximum charge-current in CC-Phase	V _{SENS}		125		mV
Tolerance of charge termination voltage	Each cell	V _{LDIFF}	0	30	50	mV
Overload-threshold Motor-shunt	Switch closed, Pin LAST	V _{LASTMAX}	40	55	70	mV
Short-circuit-threshold Motor-shunt	Switch closed, Pin LAST	U _{LASTSHORT}	200	265	350	mV
Switch Input TAST Input-Voltage HIGH Input-Voltage LOW Hysteresis		V _{IN_HIGH} V _{IN_LOW} V _{HYST}	1,8 0,8		3,5 2,5	V V V
Pull-Up Input Current	V _{IN} = 1V, LOW, V(V2) = 6V	I _{PU}		1,4		mA
Charge supply detection voltage	V _{VIN} >V _{VBAT} +V _{NT}	V _{NT}	0,5	0,9	2	V
Battery detection voltage		V _{SHORT}	0,8	1,15	1,6	V
Voltage regulator VDDA	VDDA enabled	V _{VDDA}	2,39	2,4	2,41	V
Voltage regulator VDD	V _{VBAT} =V _{VIN} =15V	V _{VDD}	2,5	3,6	4,5	V
Regulator output current VDDA	I _{VDDA} =1mA	ΔV _{VDDA}	2	6	10	mV
Regulator output current VDD	V _{VBAT} =V _{VIN} =15V, VDD=2V	I _{VDD}	2	3,5	6	mA
Logical Output SD: Output voltage High: Output voltage Low:	Output current 1 mA Output current -1mA	V _{SD_H} V _{SD_L}	2,3 0,0		2,4 0,1	V V
LED-Current LED1, LED2	Each LED- Output	I _{LED}	6	10	15	mA
Standby current consumption	VDDA disabled	I _{STBY}	0	1	3	μA
Lower operating temperature threshold	V _{VDDA} =2,4V	V _{T1}	2,19	2,23	2,27	V
Lower charging temperature threshold	V _{VDDA} =2,4V	V _{T2}	1,97	2,06	2,13	V
Upper charging temperature threshold	V _{VDDA} =2,4V	V _{T3}	0,82	0,93	1,04	V
Upper operating temperature threshold	V _{VDDA} =2,4V	V _{T4}	0,48	0,55	0,63	V
Load-resistor of Voltage-divider	Register SCHWD = High	R _{LAST}	180	230	270	kΩ

5 Timing

Supply voltage $V_{VIN}=25V$; $f_{osc} = 4,2MHz$, Temperature = $27^{\circ}C$

Parameter	Condition	Symbol	min	typ	max	Unit
Cell voltage check interval for recharge	Charge supply stays connected after charging is terminated	T_{NL}		9		min
LED on-time		T_{LED}		24		sek
Abschaltintervall (Unterspannung / Temperaturüber- / - unterschreitung)		T_{OFF}		6		sek
Load cut-off delay at overload condition	$V(\text{Load}) > V_{LASTMAX}$	T_{OL}		1,2		sek
Clock-period of overload cut-off timer		T_{CL_LOAD}		62,5		msek
Load cut-off delay at short-circuit condition	$V(\text{Load}) > 5 \times V_{LASTMAX}$	T_{SC}		300		μ sek
Charge timeout		T_{TO}		24		h
Timeout at charging with battery defect	Battery error detected	T_{TO_DEF}		17		min
Oscillator frequency in active mode	OSCENB=1, R7=270k Ω	f_{OSCA}	3,65	4,2	4,83	MHz
Oscillator frequency in standby mode	OSCENB=0	f_{OSCS}	4	12	36	KHz
LED flash frequency „slow“	Temperature error, Battery error	f_{LEDS}		0,5		Hz
LED flash frequency „fast“	Charging, Timeout error, Overload	f_{LEDF}		2		Hz
Load off after charge supply is connected	Load on	T_{OFF_NT}		28	40	msek

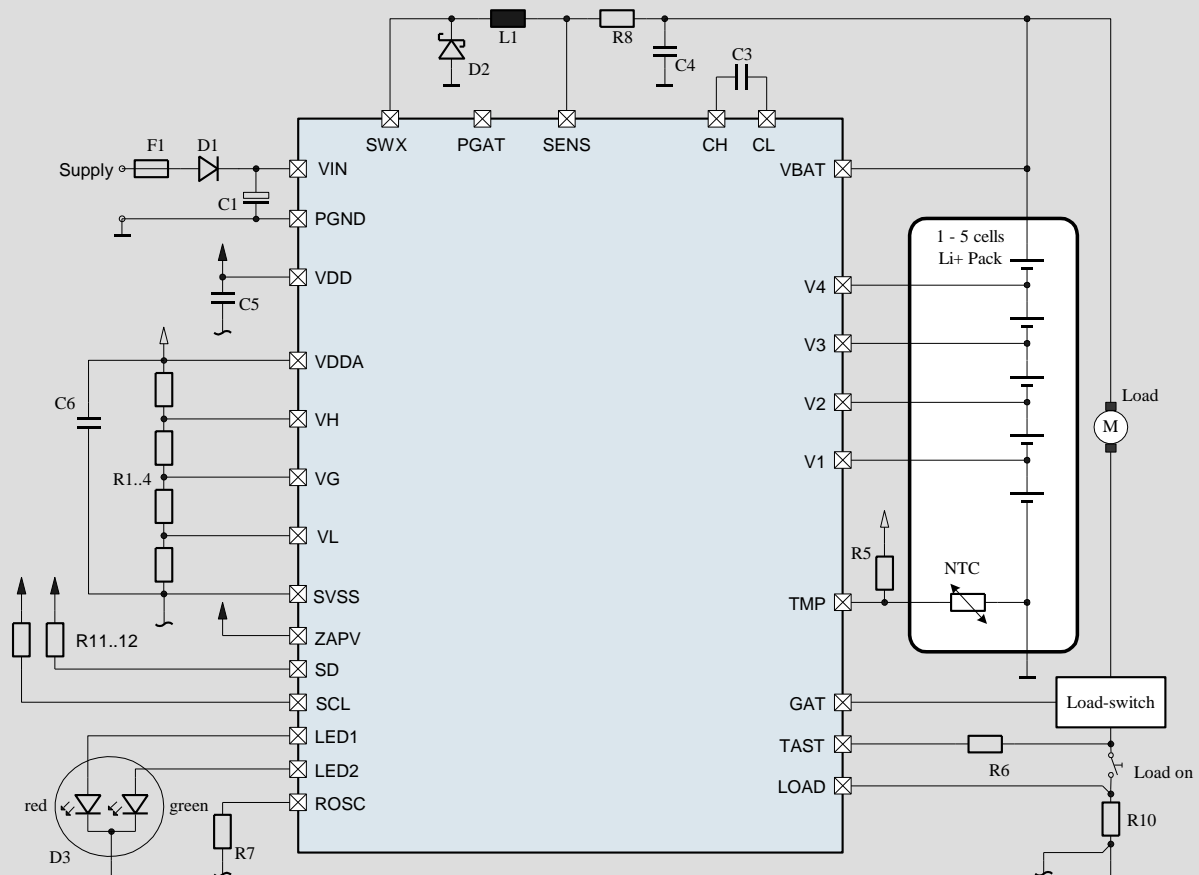
6 Application-Notes and Examples

When implementing the 701.65s down converter, the designer has to keep EMC in mind. Traces to the external parts have to be short due to the high switching frequency of approximately 500 KHz. The input capacitor has to be placed near the VIN-Pin, the freewheeling diode has to be placed near the SWX pin. The ground-connections of the input and output capacitor and the diode have to be routed very shortly and star-shaped. Connect the PGND-pin to the star-point.

The second ground-connection-pin SVSS is used for the analog components. Tie C5, C6 und the resistor-divider R1 to R4 to SVSS and R10 via a Kelvin contact to SVSS. If no load-shunt is used, connect SVSS with PGND.

6.1 Application Example Stand-Alone with 5-Cell-Battery

This example shows usage of all of the 701.65's features:

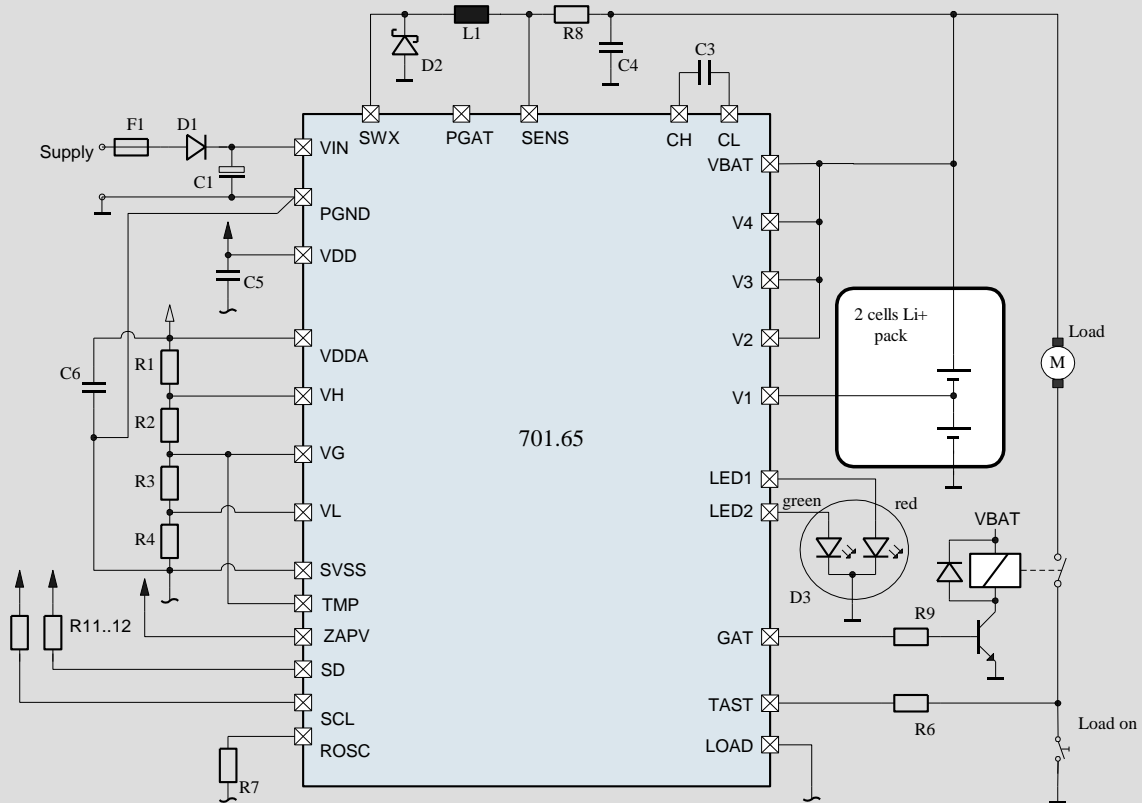


- C1: 10 μ F, 35V X5R/X7R
- C3: 220nF, 50V
- C4: 10 μ F, 35V
- C5: 1 μ F, 10V
- C6: 10 μ F, 10V
- D1: diode against reverse polarity and short-circuit
- D2: Schottky, 1A
- D3: DUO-LED Red / Green
- F1: Fuse fast blow 1A
- L1: 47 – 68 μ H, 1A
- R1..4: for dimensioning see chapter 6.3, 0,1% accuracy
- R5: 4k7 Ω
- R6: 1 k Ω
- R7: 270 k Ω
- R8: min. 250 m Ω
- R10: according to load, for dimensioning see chapter 1.8.3
- R11..12: 47 k Ω

6.2 Application example Stand-Alone, 2 cells, without temperature- and load-monitoring

This example shows the 701.65's usage with a 2-cell-Li-Ion battery without temperature- and load-monitoring. The load can be cut off with a relay.

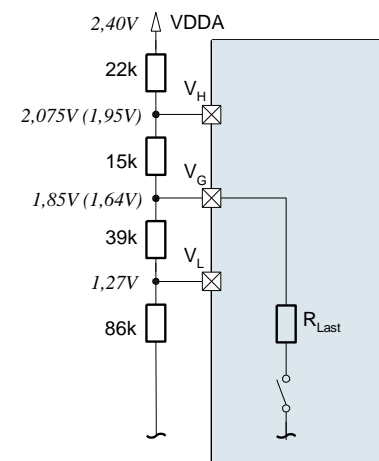
Note that TEMP is connected to VG to get a valid voltage at TEMP without the NTC. SVSS and PGND are connected with a Kelvin-contact near PGND.



- C1: 10 μ F, 35V X5R/X7R
- C3: 220nF, 50V
- C4: 10 μ F, 16V
- C5: 1 μ F, 10V
- C6: 10 μ F, 10V
- D1: diode against reverse polarity and short-circuit
- D2: Schottky, 1A
- D3: DUO-LED Red / Green
- F1: Fuse fast blow 1A
- L1: 47 – 68 μ H, 1A
- R1..4: For dimensioning see chapter 6.3, accuracy 0.1 %
- R6: 1 k Ω
- R7: 270 k Ω
- R8: min. 250 m Ω
- R9: 10 k Ω
- R11..12: 47 k Ω

6.3 Dimensioning the resistive-divider

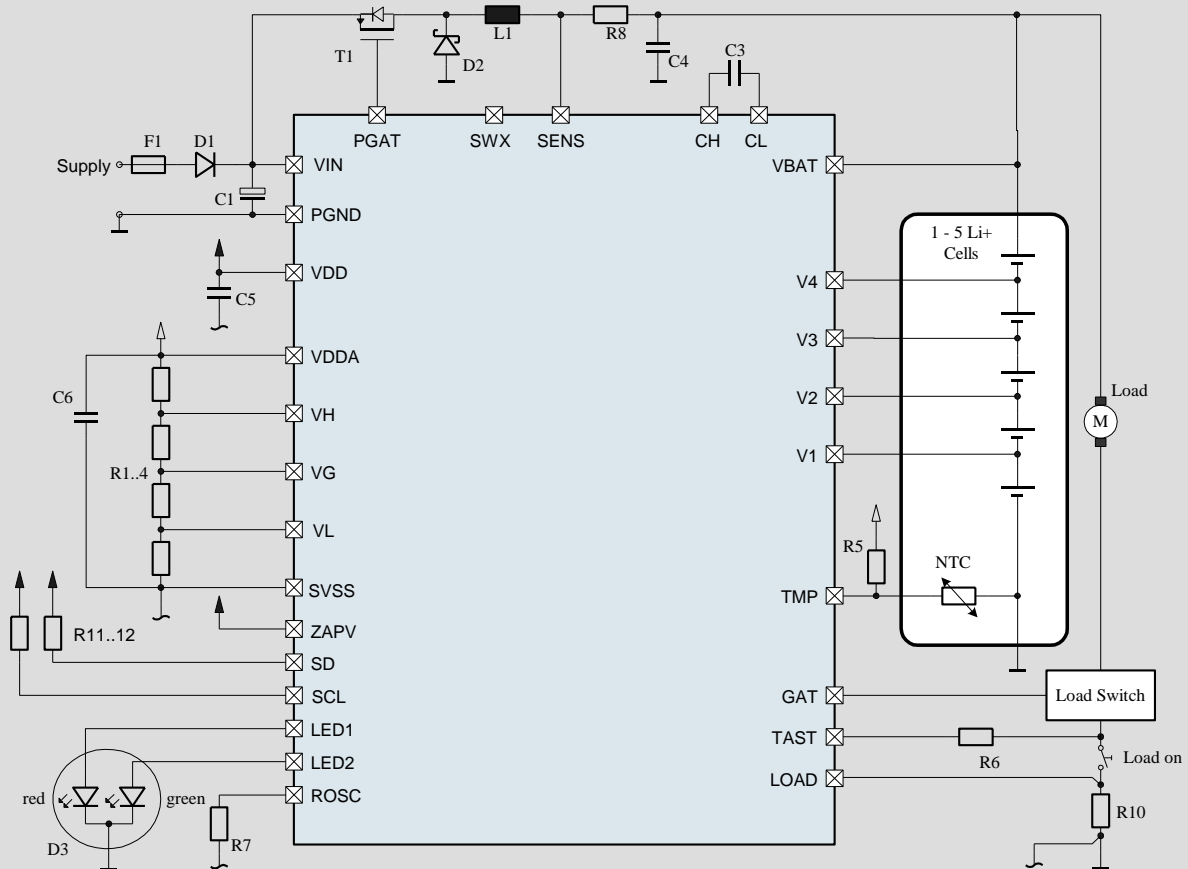
The following example shows a resistor divider for Li-Ion-Cells:



- Charge termination volt.: $V_{MAX} = 4,15V$
- Charge begins voltage: $V_{FULL} = 3,9V$
- Recharge limit: $V_{NL} = 3,7V$
- Recharge notification: $V_{YELLOW} = 3,3V$
- Minimum cell voltage: $V_{MIN} = 2,55V$

6.4 High Current (3A charge-current) Application with 5 Cells

This application utilizes an external P-MOSFET for the DC-DC-buck converter. Thru the value of the shunt R8 and an appropriate MOSFET T1, charging current may be adjusted in a wide range.



- C1: 47 μ F, 35V X5R/X7R
- C3: 220nF, 50V
- C4: 10 μ F, 25V
- C5,7: 1 μ F, 10V
- C6: 10 μ F, 10V
- D1: Diode against reverse polarity, 3A
- D2: Schottky, 4A
- D3: DUO-LED red / green 4mA
- F1: Fuse fast action 3A
- L1: 47 – 68 μ H, 4A
- R1..4: For dimensioning see chapter 6.3, Accuracy 0.1 %
- R5,11,12: 4k7
- R6: 1k Ω
- R7: 270k Ω
- R8: 39 m Ω
- R10: according to Motor-Load, Dimensioning see chapter 1.8.3
- NTC: 6K8@25 $^{\circ}$ C, z.B. Vishay 2381 640 6 3682
- T1: P-Channel MOSFET 30V, low Q_{GD}

7 Packaging

Identifier: SO-28, QFN-32 7 x 7
 Pins: lead free
 Solder ability according to IPC/JEDEC J-STD-020C

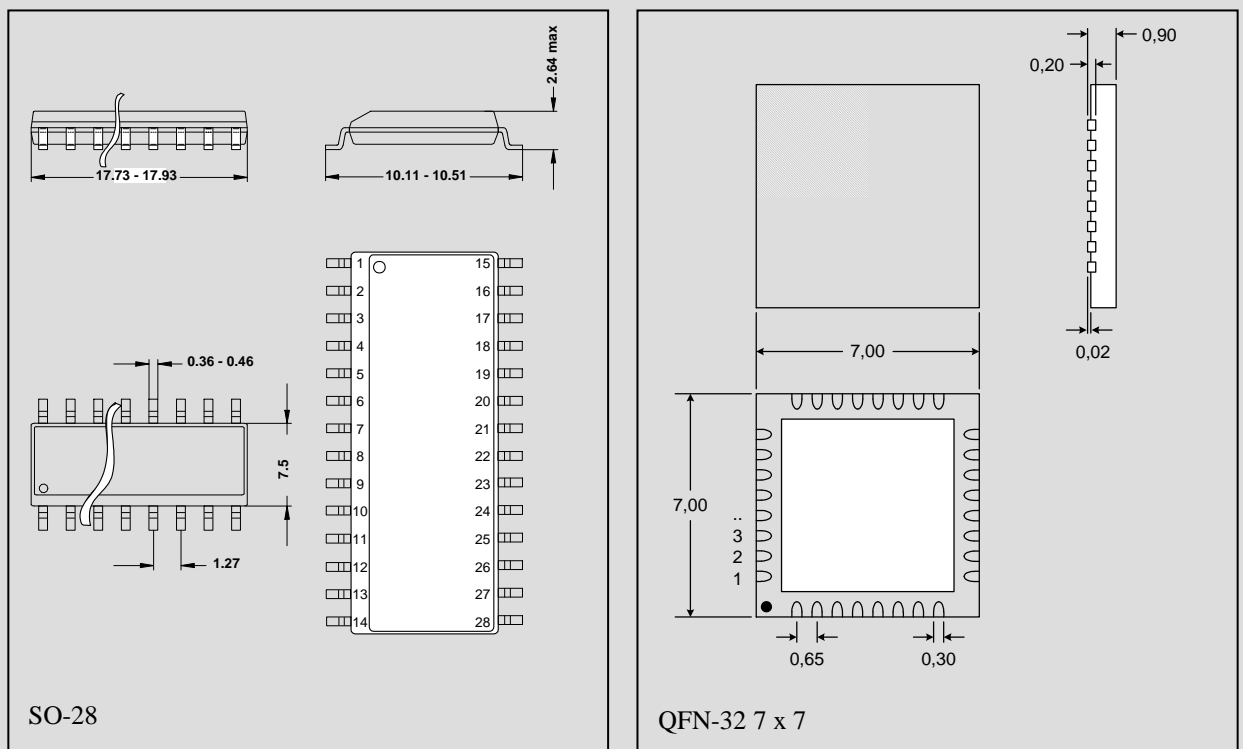
Thermal Resistance Θ_{JA} :

SO-28: 53.7 – 58.6K/W.

QFN-32: 15.5K/W.

Thermal resistance of QFN-packaging is only valid if the cooling pad is connected with 25 vias to cooling surface at other side of PCB.

7.1 Dimension



7.2 Marking

1st line: Neutron
 2nd line: Nu701.65A
 3rd line: intern

8 Revision (Rev.)

Rev.	Date	Name	Comment
1.0	18.11.10	RR	

Individual characteristics of the chip, which do not harm the function, may differ from this data sheet. These differences do not entitle the customer to claim amendment. The data sheet may be changed accordingly.